Mohammedali Khalaf

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Education

Dalhousie University — Halifax, NS, Canada
Bachelor of Electrical and Computer Engineering — *Sep. 2020 – Jun. 2025*

Experience

Undergraduate Research Assistant — May 2022 – Apr. 2025
Dalhousie Underwater Communications Laboratory: Underwater Acoustics — *Halifax, NS*

- Implemented embedded firmware on a Zynq SoC FPGA to establish SPI based data streaming between FPGA and host-computer, enabling real-time monitoring of diagnostic data
- Created system-level test cases for a Zynq FPGA based ultrasound signal transceiver to ensure functional requirements, meeting 100% code coverage.
- Designed VHDL modules for an FPGA based reciever to interface with an external ADC, enabling real time processing of signal data
- Remodeled an FPGA based signal transmitter, overseeing the entire FPGA design cycle from system modeling to VHDL implementation

Embedded Logic and Firmware Intern — Jan. 2024 – Aug. 2024
ASML Holding B.V.: Semiconductor Manufacturing Machines — *Veldhoven, Netherlands*

- Enhanced silicon wafer production efficiency of ASML EUV machines by addressing a bottleneck in the data-rate of an FPGA based data acquisition system for laser light generation.
- Wrote a mathematical model describing system data-rate limits and prepared an automated hardware test bench, enabling evaluations of current and future versions of the system in hardware.
- Proposed and implemented several HDL firmware modifications to enable higher data rates, enabling up to 270% of the defined target.
- Created an automated data processing script in Python to accelerate the analysis of raw test data and generate insights, streamlining both the research project, and several other parallel projects regarding the same device.

Electrical Engineering Intern — Jan. 2023 – Apr. 2023
Geospectrum Technologies: Underwater Acoustics — *Halifax, NS*

- Pioneered the development of a proof-of-concept communication abstraction layer in Python, enabling the software engineering team to effortlessly interact with diverse hardware components by using simplified commands.
- Provided comprehensive documentation for key stakeholders to enhance collaboration and streamline future development.

Projects

Graduation Project: Optimization of FPGA based Beamformer | *Verilog, Python* — Sep. 2024 – Apr. 2025

- Designed a system architecture of a beamforming multiplexer, enabling a wider field of view and 400% increase resolution for an existing Medical Ultrasound beamformer.
- Developed the Verilog HDL design for an FPGA based controller for the Multiplexer, allowing for system reconfiguration via SPI communications
- Utilized a combination of SystemVerilog simulations, logic analyzers, and oscilloscopes to verify system functionality, and drive system integration.
- Designed a GUI using Python to allow for fast system reconfiguration and user friendly controls

AI Based Under water Adaptive Modulation | *Python, Keras, Pandas, Matplotlib* — Sep. 2023 – Dec. 2023

- Designed a proof-of-concept architecture for an underwater communication system that uses machine learning to adapt to varying channel conditions.

Technical Skills

Languages: C, C++, VHDL, Verilog, System Verilog, Python, Tcl, MATLAB, Assembly
Programming Libraries: Keras, Sci-Kit-Learn, Pandas, NumPy, SciPy, Matplotlib, Pyserial
Communication Protocols: SPI, I2C, UART, RS-232, AXI
Software Tools: Xilinx Vivado, Altera Quartus, Lattice Diamond, LTSPICE, Ubuntu, Peta Linux, Jira, Bitbucket, Github, Confluence
Testbench Tools: Oscilloscope, Logic Analyzer, Multimeter, DC Power Supply, Function Generator